REMARKS

This application has been reviewed in light of the final Office Action dated July 13, 2007. Claims 1-40 are pending in this application, with claims 1, 9, 17, 25, 29, 33 and 37-39 being in independent form.

Claims 1, 9, 17, 25, 29, 33 and 37-40 were rejected under 35 U.S.C. §103(a) as allegedly unpatentable over Yoichiro et al. (JP06-317616) in view of U.S. Patent No. 5,481,469 to Brasen et al. Claims 2-8, 10-16, 18-23, 26-28, 30-32 and 34-36 were rejected under 35 U.S.C. §103(a) as allegedly unpatentable over Yoichiro in view of Brasen and further in view of Microsoft Press Computer Dictionary, 1997 edition.

Applicant has carefully considered the Examiner's comments and the cited art, and respectfully submits that independent claims 1, 9, 17, 25, 29, 33 and 37-39 are patentable over the cited art, for at least the following reasons.

This application relates to estimation of electric power consumption by integrated circuits which include mega cells as well as basic cells. Applicant devised an improved approach which includes estimating the electric power consumed by mega cells, which is a portion of the total power consumed by the integrated circuit.

Estimation of electric power consumed by the mega cells includes estimating the current consumed by the mega cells by (a) simulating logic states for each mega cell, (b) determining an average operation frequency for each logic state, and (c) determining an alternating current component and a direct current component for each logic state to calculate the current consumed by the mega cells. Each of independent claims 1, 9, 17, 25, 29, 33, and 37-39 addresses these features, as well as additional features.

However, it is contended in the Office Action that Yoichiro teaches techniques for

estimating electric power consumed by the basic cells of an integrated circuit, and that these disclosed techniques allegedly include (i) determining an average operation frequency for each logic state and (ii) estimating a current consumed by the basic cells. The Office Action further contends that Brasen teaches determining power consumption of mega cells and that one skilled in the art would have been motivated to modify Brasen with the techniques of Yoichiro.

Applicant respectfully disagrees.

The Detailed Description section of Yoichiro (page 4 of the machine translation provided with the Office Action), which was cited in the Office Action, states as follows:

> [0016] In drawing 2, AC power consumption value area which is the 1st storage means which stored AC power consumption value with which 201 is consumed by the component for every condition of the component for every component, and 202 are drawings having shown AC power consumption value register which is the 2nd storage means which stores the total value of AC power consumption value consumed at the present simulation time of day. And DC power consumption value area which is the 3rd storage means which stored DC power consumption value with which 203 is consumed by the component for every condition of the component for every component, and 204 are drawings having shown DC power consumption value register which is the 4th storage means which stores the total value of DC power consumption value currently consumed at the present simulation time of day.

Yoichiro, [0016] (as well as other portions), as understood by Applicant, merely states that the AC and DC power consumption values for each condition of each component of the digital circuit is determined and that these values are then added to determine a total AC power consumption and a total DC power consumption.

Accordingly, Yoichiro, contrary to the contention in the Office Action, clearly does not teach or suggest (i) determining an ***average operation frequency*** for each logic state, and (ii) estimating a ***current*** consumed by the basic cells, as provided by the subject matter of claim 1 of this application.

Moreover, Yoichiro, as acknowledged in the Office Action (as well as previously in the

record), does not teach or suggest estimating a first value of electric power consumed by ***mega cells*** of an integrated circuit based on logic simulations and pre-established power consumption data, including estimating a ***current consumed by the mega cells*** by (a) obtaining logic states for each mega cell, (b) determining an average operation frequency for each logic state, and (c) determining an alternating current component and a direct current component for each logic state to calculate the current consumed by the mega cells.

Brasen, as understood by Applicant, proposes an approach for automatic power vector generation for sequential circuits which produces input vectors for a power simulation for calculating power dissipation of logical elements (but not mega cells).

As previously discussed in the record, block BLOCK2 (see Figs. 7 and 8) is the sole disclosure in Brasen of a mega cell. Brasen states that the mega cell is a RAM or ROM which has "fixed power requirements". Since Brasen states that the mega cell described therein has fixed power requirements, one skilled in the art would not understand Brasen to be teaching or suggesting that logic simulation (to determine the logic states for each mega cell) and the ***average operation frequency for each state*** is needed to estimate the current consumed by the mega cell.

Accordingly, Brasen, like Yoichiro, fails to teach or suggest estimation of electric power consumption of an integrated circuit, which include, amongst other acts, estimating a current consumed by the mega cells by obtaining logic states for each mega cell, determining an average operation frequency for each logic state, and determining an alternating current component and a direct current component for each logic state to calculate the current consumed by the mega cells.

The Office Action cites the Microsoft Press Computer Dictionary as purportedly

proposing use of various computer readable media for storing executable code.

Applicant does not find teaching or suggestion in the cited art, however, of a computer readable medium including computer executable code stored thereon which is executable by a processor to perform a method for estimating power consumption of an integrated circuit, which comprises (a) estimating a first value of electric power consumed by the mega cells based on the logic simulations and pre-established power consumption data, including estimating a current consumed by the mega cells by obtaining logic states for each mega cell, determining an average operation frequency for each logic state, and determining an alternating current component and a direct current component for each logic state to calculate the current consumed by the mega cells, (b) estimating a second value of electric power consumed by the basic cells based on the logic simulations and pre-established power consumption data, including estimating a current consumed by the basic cells, and (c) combining the first and second values to obtain the power consumption of the integrated circuit, as provided by the subject matter of independent claim 1 of the present application.

Independent claims 9, 17, 25, 29, 33 and 37-39 are patentably distinct from the cited art for at least similar reasons.

Accordingly, for at least the above-stated reasons, Applicant respectfully submits that independent claims 1, 9, 17, 25, 29, 33 and 37-39, and the claims depending therefrom, are patentable over the cited art.

In view of the remarks hereinabove, Applicant submits that the application is now in condition for allowance, and earnestly solicits the allowance of the application.

If a petition for an extension of time is required to make this response timely, this paper should be considered to be such a petition. The Patent office is hereby authorized to charge any

fees that may be required in connection with this Response and to credit any overpayment to our Deposit Account No. 03-3125.

If a telephone interview could advance the prosecution of this application, the Examiner is respectfully requested to call the undersigned attorney.

Respectfully submitted,

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